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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,003	02/14/2002	Warren Stuart Crippen	2207/12663	6656
23838	7590	02/23/2004	EXAMINER	
KENYON & KENYON 1500 K STREET, N.W., SUITE 700 WASHINGTON, DC 20005			PATEL, ISHWARBHAI B	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/074,003	Applicant(s) CRIPPEN, WARREN STUART	
	Examiner Ishwar (I. B.) Patel	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on January 15, 2004 (RCE).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 May 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 15, 2004 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 10 -17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 10, 14 and 16, the new limitation "the contacts comprising land grid array side contacts having dimensions and spacing in the order of mils, and semiconductor side contacts having dimensions and spacing in the order of microns" is confusing.

It is unclear to the examiner as to what is claimed by "the dimension and spacing in the order mils and microns" without specifically claiming the size of the contacts and

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particularly without clarifying the spacing, either space between the contacts or space between the center of the contacts, as "mil" (inch system) and "micron" (metric system) is merely a way of specifying the dimensions.

Further, it is unclear as to what structural limitations are claimed by "grid array side contacts and semiconductor side contacts".

Additionally, regarding claim 14, the structural relations of the new limitation "the contacts comprising land grid array side contacts having dimensions and spacing in the order of mils, and semiconductor side contacts having dimensions and spacing in the order of microns" with the first silicon layer and the second silicon layer is unclear.

The specification discloses the relation of the contacts with dimensions and spacing on one side of the space transformer to that of the other side of the space transformer.

Claims 11-13, 15 and 17 depend upon claims 10, 14 and 16 and inherit same deficiency.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Claims 10-12, 14 and 16, as understood by the examiner in view of 112, second paragraph rejection, are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Pham et al., US Patent No. 6,303,992, hereafter Van, in view of Eldridge et al., US Patent No. 5,974,662.

Regarding claim 10, Van discloses a space transformer comprising:

a silicon medium (interposer body 12 made of ceramic material such a silicon, see figure 4, column 3, line 40-45; and

a predetermined contact pattern comprising electrically conductive material disposed in an inner region of the substrate and defining electrical contact zones located to provide double sided electrical contacts for the space transformer (contact pads 18 and 20 with conductive conduits 22, see figure 4, column 3, line 1-8), but

fails to explicitly disclose the contacts comprising land grid array side contacts having dimensions and spacing in the order of mils, and semiconductor side contacts having dimensions and spacing in the order of microns.

Though, Van discloses a space transformer 12 with semiconductor die 50 connected on one side of the space transformer 12 and a substrate 70 on the other side, with narrower pitch between the contacts on semiconductor side and contacts on the substrate side distributed in larger area, see figure 4, column 3, line 40-65.

Eldridge discloses a space transformed 400 with top surface 402a with a relatively fine pitch, about 5-10 mil pitch, center to center spacing comparable to semiconductor die bond pad and bottom surface 402b with terminals at a 50-100 mil pitch, comparable to printed circuit board pitch, see column 23, line 5-25.

A person of ordinary skill in the art at the time the invention was made would readily construe that the spacing on the semiconductor side of a space transformer would be in microns, with narrower pitch, and that on the printed wiring board side would be in mils, with wider pitch, for connecting a semiconductor device on one side of the space transformer and a printed circuit board on the other side of the board.

Furthermore, space transformers / interposers, as evident from Van and Eldridge, are adapted to have semiconductor device, with contacts at narrower pitch, to be connected on one side and a printed circuit board, with contacts at wider pitch, to be connected on the other side, and to specify the pitch in mil (inch system) and in micron (metric system) is merely a way of specifying the dimensions.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to construe, the dimension / spacing between the contacts on surfaces of the space transformer of Van in the order of mils, with wider pitch, on land grid array side, and in the order of microns, with narrower pitch, on semiconductor side, from the teachings of Eldridge, in order to connect the semiconductor device on one side and the printed circuit board on the other side.

Regarding claim 11, the body of Van further discloses a first and second silicon layer with contact pattern being disposed between the first silicon layer and second silicon layer, see figure 4 and 8A-B, column 4, line 60 to column 5, line 5.

Regarding claim 12, the body of Van further discloses the via with electrically conductive material into the via (see figure 4, column 4, line 1-5).

Regarding claim 14, the modified circuit board of Van discloses all the features of the claimed invention, as applied to claim 10-12 above, including the contact pattern comprising copper, column 4, line 1-10.

Regarding claim 16 and 17, the modified circuit board of Van discloses all the features of the claimed invention, as applied to claim 10-12 above, including the means disposed in an inner region located between the first silicon layer and the second silicon layer, electrically conductive conduits 22, see figure 4, column 3, line 65 to column 4, line 10.

6. Claims 13 and 15, as best understood by the examiner in view of 112, second paragraph rejection above, are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Van and Eldridge, as applied to claims 10-12 above, and further

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in view of Petrarca et al., US Patent No. 6,429,522, hereafter, Petrarca and Matsuo et al., US Patent No. 6,614,106, hereafter, Matsuo.

Regarding claim 13, the combination of Van and Eldridge discloses all the features of the claimed invention as applied to claims 10-12 above, but

fails to disclose an adhesion promoter disposed between the electrically conductive material and the first silicon layer.

Petrarca, in the background discussion, discloses that it is known in the semiconductor industry to apply an adhesion promotion layer such as silicon oxide, silicon nitride, titanium, tungsten or related compounds, before a metal deposition. The adhesion promotion layer is often used as a barrier for metal migration.

Matsuo discloses an interposer 30 made out of silicon substrate, column 2, line 35-50, and adhesion promotion layer for copper plating, column 3, line 23-30.

A person of ordinary skill in the art would readily recognize the advantage of providing adhesion promotion layer, before metal deposition, for better adhesion of the metal.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified structure of Van with adhesion promotion layer, from the teachings of Petrarca and Matsuo, in order to have better adhesion of the metal deposition.

Response to Arguments

7. Applicant's arguments with respect to claims 10-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mashino discloses an interposer, which can made of silicon substrate, column 3, line 17-30, with semiconductor chip 34 connected on one side and a circuit board connected on the other side, see figure 5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



I B Patel
Examiner
GAU: 2827
February 2, 2004